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Invention Name: a voltage reference signal line layout of the multi-layer substrate

Invention Summary

A kind of voltage reference signal line layout of the multi-layer substrates, mainly in the signal level voltage reference signal to other non-Xian Lu pull signal layer layout, then layer the signal makes the signal more access lines in the layout space, rather than signal layer voltage reference signal line not only will not be the signal line coupling noise interference, and can have a great layout flexibility. In addition, the voltage reference signal circuit design of wire width can be used to improve its parasitic resistance.

Invention

This invention is a kind of voltage reference signal on the line layout (layout) of the multi-layer substrate, and in particular there is a way to signal line configuration on the signal level, while the voltage reference signal line configuration in the other layer (power planes, ground floor) The multi-layer substrate.

In general logic circuit chips, or large-scale integrated circuit, a voltage reference signal (Voltage reference signal, Vref) to the same group as the signal voltage to determine the standards by which to judge the logic signal is high or low of bit standard position, to facilitate computing and digital signal processing. Therefore, the voltage reference signal must be maintained at a certain voltage level, try to avoid interference with other signals, noise coupling (coupling) resulting voltage to the float (voltage variation). Once around the voltage reference signal interference caused by signals flowing, it will result in other digital logic signal is not normally a voltage signal as a standard reference for interpretation, it would make data interpretation error, serious, or even the whole system will not function properly Ling. Therefore, how to maintain the voltage reference signal of the signal integrity (signal integrity), and thus avoid the voltage reference signal coupled by the noise interference of other signals will be very important work.

First of all, refer to Figure 1, the painting shows four plates for the most traditional section diagram. General package substrate (substrate) or printed circuit board (PrintedCircuit Board, PCB) is usually a four-layer board 100. Four-layer board 100 mainly by the signal layer 104, ground layer 108, the power layer 112 and the signal layer 116 into a ditch.

Signal level between 104 and 108 ground floor is equipped with insulation layer 106, ground layer and power layer 108 is equipped with insulation layer between 112 110 and 112 and the signal layer power planes equipped with insulation layer between 116

114. In addition, the signal layer 104 and the signal layer 116 also is equipped with welded outer cover layer 102 and solder mask layer 118.

Signal layer 104 and the signal layer 116 of the line system as the signal input / output purposes, all the signals are signals from the signal layer 104 and layer 116 to input / output actions, and the signal level between 104 and 116 will signal layer by plug (not shown painted) electrically connected to each other.

Then please refer to Figure 2, the painting shows the signal level for the study to know the voltage reference signal circuit layout diagram. Signal layer layout of the main circuit voltage reference signal by the voltage reference signal composed of lines and signal lines. Located on the insulating layer 106 to the signal layer 104, for example, the signal layer 104 of the voltage reference signal line layout mainly by the voltage reference signal line 104a and 104b which constitute the signal line, while the voltage reference signal line 104a and the signal line 104b will be by plug 120 and the signal layer 116 (shown in drawing figure 1) electrical connection. The voltage reference signal line 104a of the signal often affected by other signal line 104b of the coupling noise interference, and then makes the voltage reference signal line 104a flowing in the signal generation phenomenon, can not maintain a steady voltage.

Then please refer to Figure 3, the painting shows the signal level for the study to know the voltage reference signal circuit layout diagram. 3 figure dwarfed the voltage reference signal line shows the layout diagram with 2 similar, the difference lies in the signal line 104b and the voltage reference signal of double spacing between lines 104a (doublespacing) designed to reduce the signal line 104b of the voltage reference signal line 104a of the coupling noise caused by interference. However, Fig 3 the voltage reference signal circuit layout are still not allowed to solve the electromagnetic field caused by the coupling effect of noise interference and signal level in the layout space of the case, the designer is bound to interference with the layout of the coupling Zaxun compromise between space.

Therefore, the purpose of the present invention has a voltage reference signal is proposed layout of the multi-layer circuit board, can effectively avoid the voltage reference signal line and signal line coupling between the noise interference.

To achieve this purpose the invention proposes a voltage reference signal with the layout of the multi-layer circuit substrate, mainly to the voltage reference signal layer line pull signals to other non-signal layer layout, and then make the signal level of the signal line with larger layout space, rather than the signal level in the voltage reference signal line not only will not be the signal line coupling noise interference, and can have a great layout flexibility. In addition, the voltage reference signal circuit design of wire

width can be used to improve its parasitic resistance.

The invention has the voltage reference signal line layout of the multi-layer substrate such as a first signal by the level, a number of plug, a ground layer, a power layer and a second signal layer composition, plug, ground layer and power layer such as system configuration on the first signal layer and the second signal layer. Among them, the first signal layer such as line voltage reference signal from the first line and a number of signal lines that constitute, for example, by the power level of a second voltage reference signal line and and a patterned conductor layer composed of some of the plug Cyprus to be the first signal line layer and the second signal layer electrically connected, part of the plug system to be the first voltage reference signal line voltage reference signal line and the second electrical connection, while most of the plug line voltage reference signal to the second signal line and the second electrical connection layer.

The invention has the voltage reference signal line layout of the multi-layer substrate, the first signal layer, ground level, power level and the second signal layer between the layers are configured with a dielectric layer, while the outer layer of the invention in the first signal and the second external signal layer has a solder mask layer configuration.

The invention has the voltage reference signal line layout of the multi-layer substrate, in the ground layer and power layer can be configured to at least one signal layer, the first signal layer and ground layer can be configured for a ground - the signal level, while in the second between the signal layer and power layer can also configure a power supply - the signal level.

The invention has the voltage reference signal line layout of the multi-layer substrate such as a first signal by the level, a number of plug, a non-signal layer and a second signal layer composition, plug and non-signal layers such as system configuration in the first signal layer and the second signal layer. Among them, the first signal layer such as line voltage reference signal from the first line and a number of signal lines that constitute, for example, by the non-signal layer of a second voltage reference signal line and and a patterned conductor layer composed of some of Plug system for the first signal layer and the second signal layer electrically connected, part of the plug system to be the first voltage reference signal line voltage reference signal line and the second electrical connection, while most of insertion Cyprus Department of voltage reference signal to the second signal line and the second electrical connection layer.

The invention has the voltage reference signal line layout of the multi-layer substrate, the first signal layer, non-signal layer and the second floors of the indirect signal level is equipped with a dielectric layer, and the invention of the first signal layer and the second signal layer outside the outer are equipped with a solder mask layer.

The invention has the voltage reference signal line layout of the multi-layer substrate, in the first signal layer and the non-signal layers can be configured for a ground - the signal level, while in the second signal layer and the non-signal layers can also configure a power supply - signal layer.

The invention has the voltage reference signal line layout of the multi-layer substrate such as a signal by the layer, a non-signal layer and composed of multiple plug. Among them, the signal level for example, consist of a first voltage reference signal lines and signal lines composed of multiple, non-signal layer configuration on the signal level below the non-signal layer such as a second voltage reference by the signal line and a pattern of conductor layer composition, and multiple plug configurations in the signal layer and the non-signal layer, used to plug such as the first line voltage reference signal line and the second voltage reference signal line electrically connected.

The invention has the voltage reference signal line layout of the multi-layer substrate, the signal layer and the non-signal layer is equipped with a dielectric layer, while the signal of the outer layer equipped with a welding hood.

The invention has the voltage reference signal line layout of the multi-layer substrate, the non-signal layer for example, by the power of a ground layer and a layer. In addition, the ground layer and power layer instance, it can configure at least one signal layer.

To enable the invention of the above purposes, features, and advantages can be more clearly understood, the following special give a better implementation of the legislation and with the photo-type, as detailed below:

Schema simple explanation

1 illustrations showing the most traditional section diagram of four plates;

2 illustrations show the signal level for the practice known in the voltage reference signal circuit layout diagram;

3 illustrations show the signal level for the study to know the voltage reference signal circuit layout diagram;

4 illustrations show the first embodiment in accordance with the invention of the profile diagram of four-layer board;

5 illustrations show the first embodiment in accordance with the invention of the voltage signal level reference signal circuit layout diagram;

6 illustrations, showing the first embodiment in accordance with the present invention voltage reference signal power level in the circuit layout diagram;

7 illustrations, showing the first embodiment in accordance with the present invention the signal layer and power layer overlapping the signal after the voltage reference circuit layout diagram;

8 illustrations showing the second embodiment in accordance with the invention of the profile diagram of multilayer;
9 illustrations, showing the third embodiment in accordance with the invention of the profile diagram of multilayer; and
10 illustrations, showing the fourth embodiment in accordance with the invention of the profile diagram of multilayer.
Symbol shows the main components
100,200. . . Four-layer board
102,118,202,218. . . Solder mask layer
104,116,204,216. . . Signal line layer
104a. . . Voltage reference signal line
104b, 204b. . . Signal line
106,110,114,206,210,214. . . Insulation
108,208. . . Ground floor
112,212. . . Power planes
120,220,222,224. . . Plug
204a. . . The first voltage reference signal line
226. . . The second voltage reference signal line
228. . . Patterned conductor layer
300. . . Multilayer
302,326. . . Solder mask layer
304,312,316,324. . . Signal layer
306,310,314,318,322. . . Insulation
308. . . Ground floor
320. . . Power planes
400. . . Multilayer
402,426. . . Solder mask layer
404,424. . . Signal layer
406,410,414,418,422. . . Insulation
408. . . Ground - Signal Layer
412. . . Ground floor
416. . . Power planes
420. . . Power - Signal Layer
500. . . Multilayer
502,514. . . Solder mask layer
504,512. . . Signal layer

506,510. . . Insulation

508. . . Non-signal layer

The first implementation of the cases

First of all, please refer to Figure 4, the painting shows the first embodiment in accordance with the invention of the profile diagram of four-layer board. General package substrate or printed circuit board is usually a four-layer board 200. Four-layer board 200 mainly by the signal layer 204, ground plane 208, power planes 212 and 216 constitute a signal layer.

Signal level between 204 and 208 ground floor is equipped with insulation layer 206, ground layer and power layer 208 is equipped with insulation layer between 212 210 and 212 and the signal layer power planes equipped with insulation layer between 216 214. In addition, the signal level and signal level 204 is equipped with 216 more outside the welding mask layer 202 and solder mask layer 218.

Signal layer 204 and the signal layer 216 of the line system as the signal input / output purposes, all the signals are signals from the signal layer 204 and layer 216 to input / output actions, and the signal level between 204 and 216 will signal layer by Plug (painted shown in Figure 5) electrically connected to each other.

5 illustrations show the first embodiment in accordance with the invention of the voltage signal level reference signal circuit layout diagram. Please also refer to Figure 4 and Figure 5, the signal level voltage reference signals 206,216 in the main distribution line voltage reference signal by the signal line by line and form.

Located on the insulating layer 206 to the signal layer 204, for example, the signal layer 204 of the voltage reference signal circuit layout such as by the first voltage reference signal line 204a and 204b composed of multiple signal lines. Among them, the first voltage reference signal line 204a at one end with an electrical connection plug 220, while the other signal line 204b will be held by the bottom plug 224 and the signal layer 216 electrically connected.

6 illustrations, showing the first embodiment in accordance with the invention of the voltage reference signal power level schematic circuit layout. Please also refer to Figure 4 and Figure 6, the power layer 212, for example, a second voltage reference by the signal line 226 and a patterned conductive layer 228 form. Among them, a second voltage reference signal line 226 respectively with the two ends such as plug 220, electrically connected to plug 222, while the patterned conductor layer 228 such as a 6 Figure dwarfed shows the pattern of (patterning), patterned conductor layer 228 in the second voltage reference signal line 226, plug 220, 222, and plug the regional distribution plug 224 will display the basket empty state, so the design will be able to

make patterned second conductor layer 228 will not voltage reference signal line 226, 220 Plugs, plug 222, a short circuit plug 224 of the phenomenon.

However, those familiar with the technology should be able to easily understand the position 204 in the signal layer and power layer 212 between the ground layer 208 corresponds to the plug 220, plug 222 and plug 224 showing the location of the basket will be empty state to facilitate the plug 220, 222, and plug the configuration of plug 224.

Can see from the above, four-layer board 200 in plug 220, plug 222 and plug 224 has its role. Among them, the plug 220 such systems will be the first voltage reference signal line 204a and the second voltage reference signal line 226 electrically connected, plug 220 such systems will be the second voltage reference signal line 226 and 216 electrically connected to the signal layer, and insert Cyprus Department of the signal layer 224 such as 204 and 216 electrically connected to the signal layer.

7 illustrations, showing the first embodiment in accordance with the present invention the signal layer and power layer overlapping the signal after the voltage reference circuit layout diagram. Please also refer to Figure 4 and Figure 7, the signal layer and power layer 212, 204 overlap, you can clear that the second voltage reference signal line 226 to one end by plug 220 and the first power voltage reference signal line 204a of connection, and the second voltage reference signal line 226 to the other end through the bottom plug 222 and 216 electrically connected to the signal layer.

The first voltage reference signal line 204a and the second voltage reference signal line 226, which form a complete circuit voltage reference signal. As the second voltage reference signal line 226 in the power layer 212, while in the power layer 212 and signal ground plane between the layers 204 208 electromagnetic shielding effect, which can greatly reduce the voltage reference signal line and the other signal lines of coupling between the noise interference, and further makes the voltage reference signal line 204a of the signal maintained at a stable voltage.

Signal layer 204 of the voltage reference signal line 212 in Latin America to the power layout layer, and then makes the signal layer 204 of the signal line 204b has a larger layout space, and the second voltage reference signal line 226 itself also has a considerable layout flexibility. In addition, the second voltage reference signal line 226, the design of wire width can be used to improve their parasitic resistance problems.

However, those familiar with the technology should be able to easily understand the signal layer 204, the voltage reference signal line 208 in Latin America to the ground floor layout is also a practical way. This layout also can increase the signal line 204b of the layout of space, and voltage reference signal line itself, the layout flexibility.

Second embodiment

Please refer to Figure 8, the painting shows the second embodiment in accordance with the invention of the profile diagram of multilayer. The invention circuit voltage reference signal is not only used in the layout of the concept of four plates, which can also be applied to multilayer board. The implementation of the case, multiply mainly by the signal level of 300 304, ground layer 308, the signal layer 312, the signal layer 316, power planes 320 and 324 constitute a signal layer. Signal level between 304 and 308 ground floor is equipped with insulation layer 306, ground plane 308 and signal layer 312 is equipped with insulation layer between the 310, the signal layer 312 and the signal layer 316 is equipped with insulation between the 314, 316 and power signal level layer 320 is equipped with insulation layer between 318 and 320 and the signal layer power planes equipped with insulation layer between 324 322. In addition, the signal level and signal level 304 is equipped with 324 more outside the welding mask layer 302 and solder mask layer 326.

The implementation of the case, the signal can be voltage reference layer 304 and pulled to the ground level signal line 308 or 320 of the power layout layer, so as to avoid coupling noise interference to enhance the purpose of layout flexibility.

Third embodiment

Please refer to Figure 9, the drawing shows the third embodiment in accordance with the invention of the profile diagram of multilayer. The implementation of the case, multiply mainly by the signal level of 400 404, ground - the signal layer 408, ground plane 412, power supply layer 416, power supply - the signal level 420 and 424 constitute a signal layer. Signal layer 404 and the ground - the signal level 408 is equipped with insulation layer between the 406, ground - the signal level between 408 and 412 ground floor is equipped with insulation layer 410, ground layer and power layer 412 is equipped with insulation layer between 416 414, power supply layer 416 and power - between the signal layer 420 is equipped with insulation layer 418, and power - the signal level between 420 and 424 equipped with the signal layer insulating layer 422. In addition, the signal layer 404 and the signal layer 424 also is equipped with solder mask outer layer 402 and solder mask layer 426.

The implementation of the case, the signal layer 404 can be the voltage reference signal line pull to the ground - the signal layer 408, ground plane 412, power level or power supply 416 - 420 in the signal layer of the layout, to be able to avoid coupling noise interference to promote the purpose of layout flexibility.

Fourth embodiment

Please refer to Figure 10, the painting shows the fourth embodiment in accordance with

the invention of the profile diagram of multilayer. The implementation of the example, multiply 500 by the signal layer 504 mainly non-signal layers 508 and 512 constitute a signal layer. Signal layer 504 and the non-signal layer 508 is equipped with insulation layer between the 506, rather than the signal level between 508 and 512 equipped with the signal layer insulating layer 510. In addition, the signal layer 504 and the outer signal layer 512 also is equipped with solder mask layer 502 and solder mask layer 514.

The implementation of the case, the signal layer 504 can be the voltage reference signal line pull to the non-signal layer 508 in the layout, to be able to avoid coupling noise interference, the purpose of enhancing flexibility in the layout.

In summary, the present invention has a voltage reference signal line layout of the multi-layer substrate, at least the following advantages:

1. The present invention has the voltage reference signal line layout of the multi-layer substrate, the voltage reference signal line may be obscured by the ground plane of the electromagnetic effect, and thus greatly reduce the voltage reference signal line and the other signal coupling noise interference between lines.

2. The present invention has the voltage reference signal line layout of the multi-layer substrate, the voltage reference signal line configuration on the signal level other than the wire layer, making voltage reference signal line greatly increased flexibility in their layout.

3. The present invention has the voltage reference signal line layout of the multi-layer substrate, the voltage reference signal line configuration on the signal level other than the wire layer, making the other signal lines in the signal layer in a large layout space.

4. The present invention has the voltage reference signal line layout of the multi-layer substrate, the voltage reference signal line configuration on the signal level other than the wire layer, can be voltage reference signal circuit design for the wide wire, in order to effectively reduce the parasitic wire resistance.

Although the invention has been implemented in order to better expose the above cases, however, its not to limit the invention, any person familiar with this technique, not from the spirit and scope of the present invention, the when can be used for a variety of changes and polish, so the present invention The scope of protection when, as the scope of the attached patent application, whichever is defined.

Claims:

1. A kind of voltage reference signal line layout of the multi-layer substrates, including: a first signal layer, the first signal layer including a first voltage reference signal line and a plurality of signal lines; a second signal layer, the configuration in the first below the signal layer; a plurality of first plug, configured in the first signal layer and the second signal layer, and the more the signal line and the second signal layer electrically connected; a ground layer, the configuration in the The first signal layer and the second signal layer; a power level, the configuration at the first signal layer and the second signal layer, the layer includes a second power supply voltage reference signal line and a patterned conductor layer ; a second plug, configured in the power layer and the first signal layer and the first voltage reference signal line and the second voltage reference signal line electrically connected; and a third plug, configure in the power layer and the second signal layer, and the second voltage reference signal line and the second signal layer electrically connected.

2. As of claim 1 has a voltage reference signal referred to the layout of the multi-layer circuit substrate, where the first signal layer, the ground floor, the power layer and between layers of the second signal layer is equipped with a dielectric layer .

3. As of claim 1 has a voltage reference signal referred to the layout of the multi-layer circuit substrate, in which the outer layer of the first signal is configured with a first solder mask layer.

4. As of claim 1 has a voltage reference signal referred to the layout of the multi-layer circuit substrate, in which the outer layer of the second signal is configured with a second solder mask layer.

5. As of claim 1 has a voltage reference signal referred to the layout of the multi-layer circuit substrate, where the ground floor level with the power configuration between the more there is a third signal level.

6. As of claim 5 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, where the ground floor level with the power configuration between the more there is a fourth signal layer.

7. As of claim 1 has a voltage reference signal referred to the layout of the multi-layer circuit substrate, where the first signal layer and the ground floor is equipped with a ground between the more - the signal level.

8. As of claim 1 has a voltage reference signal referred to the layout of the multi-layer circuit substrate, where the second signal layer and the layer of the power supply is equipped with a power greater - the signal level.

9. As of claim 1 has a voltage reference signal referred to the layout of the multi-layer circuit substrate, where the first signal layer and the ground floor is equipped with a

ground between the more - the signal level, and the second signal layer and the more configuration between power planes have a power supply - the signal level.

10. A kind of voltage reference signal line layout of the multi-layer substrates, including: a first signal layer, the first signal layer including a first voltage reference signal line and a plurality of signal lines; a second signal layer, the configuration in the first a signal level below; a plurality of first plug, configured in the first signal layer and the second signal layer, and the more the signal line and the second signal layer electrically connected; at least one non-signal layer configuration in the first signal layer and the second signal layer, the non-signal layer including a second voltage reference signal line and a patterned conductor layer; a second plug, configured in the non-signal layer and the first signal layers, and the first voltage reference signal line and the second voltage reference signal line electrically connected; and a third plug, configured in the non-signal layer and the second signal layer, and the second voltage reference signal line and the second signal layer electrically connected.

11. As of claim 10 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, where the first signal layer, the non-signal layer and between layers of the second signal layer is equipped with a dielectric layer.

12. As of claim 10 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, in which the outer layer of the first signal is configured with a first solder mask layer.

13. As of claim 10 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, in which the outer layer of the second signal is configured with a second solder mask layer.

14. As of claim 10 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, in which the non-signal layer includes a power supply layer.

15. As of claim 14 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, in which the non-signal layer including a ground layer.

16. As of claim 15 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, where the ground floor level with the power configuration between the more there is a third signal level.

17. As of claim 15 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, where the ground floor level with the power configuration between the more there is a fourth signal layer.

18. As of claim 10 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, the first signal layer and the non-signal layer also equipped with a ground - the signal level.

19. As of claim 10 with the voltage reference signal referred to the layout of the multi-layer circuit substrate, where the second signal layer and the non-signal layer also equipped with a power supply - the signal level.

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發明 新型 專利說明書

一、發明新型名稱	中文	具有電壓參考訊號線路佈局之多層基板
	英文	
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四、中文發明摘要（發明之名稱：具有電壓參考訊號線路佈局之多層基板）

一種具有電壓參考訊號線路佈局之多層基板，主要係將訊號層中的電壓參考訊號線路拉至其他非訊號層中進行佈局，進而使得訊號層中的訊號線路具有較大的佈局空間，而非訊號層中的電壓參考訊號線路不但不會受到信號線路的耦合雜訊干擾，而且能夠具有相當大的佈局彈性。此外，電壓參考訊號線路可採用寬導線的設計以改善其寄生電阻。

英文發明摘要（發明之名稱：　　）

五、發明說明（ / ）

本發明是有關於一種具有電壓參考訊號線路佈局（ layout ）之多層基板，且特別是有關於一種將訊號線路配置在訊號層，而將電壓參考訊號線路配置在其他層（電源層、接地層）之多層基板。

在一般邏輯電路晶片或是大型積體電路中，以電壓參考訊號（ Voltage reference signal，Vref ）來作爲同一群組訊號的電壓準位判定標準，藉此來判斷邏輯訊號是高準位或是低準位，以利數位訊號的運算及處理。因此，電壓參考訊號必須要維持在一定的電壓準位，盡量避免受到其他訊號的耦合雜訊干擾（ coupling ）而導致電壓準位飄動（ voltage variation ）。一旦周遭訊號的干擾造成電壓參考訊號飄動時，便會造成其他數位邏輯訊號無法正常地以電壓參考訊號爲標準進行判讀，這將會使得資料判讀錯誤，嚴重的話甚至會另整個系統無法正常運作。因此，如何維持電壓參考訊號的訊號完整度（ signal integrity ），進而避免電壓參考訊號受到其他信號的耦合雜訊干擾將是相當重要的工作。

首先請參照第 1 圖，其繪示爲習知四層板之剖面示意圖。一般的封裝基板（ substrate ）或是印刷電路板（ Printed Circuit Board，PCB ）通常爲一四層板 100。四層板 100 主要是由訊號層 104、接地層 108、電源層 112 以及訊號層 116 所構成。

訊號層 104 與接地層 108 之間配置有絕緣層 106，接地層 108 與電源層 112 之間配置有絕緣層 110，而電源層

五、發明說明（乙）

112 與訊號層 116 之間配置有絕緣層 114。此外，在訊號層 104 與訊號層 116 外更配置有焊罩層 102 與焊罩層 118。

訊號層 104 與訊號層 116 中的線路係作爲訊號的輸入/輸出之用，所有的訊號都會由訊號層 104 與訊號層 116 進行輸入/輸出的動作，且訊號層 104 與訊號層 116 之間會藉由插塞（未繪示）而彼此電性連接。

接著請參照第 2 圖，其繪示爲習知訊號層中電壓參考訊號線路佈局的示意圖。訊號層中的電壓參考訊號線路佈局主要係由電壓參考訊號線路以及訊號線路所構成。以位於絕緣層 106 上之訊號層 104 爲例，訊號層 104 中的電壓參考訊號線路佈局主要是由電壓參考訊號線路 104a 與訊號線路 104b 所構成，而電壓參考訊號線路 104a 與訊號線路 104b 則會藉由插塞 120 與訊號層 116（繪示於第 1 圖中）電性連接。上述電壓參考訊號線路 104a 中的訊號常會受到其他訊號線路 104b 的耦合雜訊干擾，進而使得電壓參考訊號線路 104a 中的訊號產生飄動的現象，無法維持穩定的電壓準位。

接著請參照第 3 圖，其繪示爲習知訊號層中電壓參考訊號線路佈局的示意圖。第 3 圖中所繪示的電壓參考訊號線路佈局與第 2 圖相似，其差異之處在於訊號線路 104b 與電壓參考訊號線路 104a 之間採用雙重間距(double spacing)的設計，以期降低訊號線路 104b 對電壓參考訊號線路 104a 所造成的耦合雜訊干擾。但是，第 3 圖中的電壓參考訊號線路佈局仍然不能完全地解決電磁場效應所造

五、發明說明（7）

成的耦合雜訊干擾，且在訊號層的佈局空間不足的情況下，設計者勢必要在耦合雜訊干擾與佈局空間之間作出妥協。

因此，本發明的目的在提出一種具有電壓參考訊號線路佈局之多層基板，能夠有效避免電壓參考訊號線路與信號線路之間的耦合雜訊干擾。

爲達本發明之上述目的，提出一種具有電壓參考訊號線路佈局之多層基板，主要係將訊號層中的電壓參考訊號線路拉至其他非訊號層中進行佈局，進而使得訊號層中的訊號線路具有較大的佈局空間，而非訊號層中的電壓參考訊號線路不但不會受到信號線路的耦合雜訊干擾，而且能夠具有相當大的佈局彈性。此外，電壓參考訊號線路可採用寬導線的設計以改善其寄生電阻。

本發明具有電壓參考訊號線路佈局之多層基板例如係由一第一訊號層、多個插塞、一接地層、一電源層以及一第二訊號層所構成，插塞、接地層以及電源層例如係配置於第一訊號層與第二訊號層之間。其中，第一訊號層例如係由一第一電壓參考訊號線路以及多個訊號線路所構成，電源層例如係由一第二電壓參考訊號線與及一圖案化導體層所構成，部份的插塞係用以將第一訊號層與第二訊號層電性連接，部份的插塞係用以將第一電壓參考訊號線路與第二電壓參考訊號線路電性連接，而部份的插塞係用以將第二電壓參考訊號線路與第二訊號層電性連接。

本發明具有電壓參考訊號線路佈局之多層基板中，

五、發明說明（4）

第一訊號層、接地層、電源層以及第二訊號層各層之間皆配置有一介電層，而本發明於第一訊號層外以及第二訊號層外接配置有一焊罩層。

本發明具有電壓參考訊號線路佈局之多層基板中，在接地層與電源層之間可配置至少一訊號層，在第一訊號層與接地層之間可配置一接地-訊號層，而在第二訊號層與電源層之間亦可配置一電源-訊號層。

本發明具有電壓參考訊號線路佈局之多層基板例如係由一第一訊號層、多個插塞、一非訊號層以及一第二訊號層所構成，插塞以及非訊號層例如係配置於第一訊號層與第二訊號層之間。其中，第一訊號層例如係由一第一電壓參考訊號線路以及多個訊號線路所構成，非訊號層例如係由一第二電壓參考訊號線與及一圖案化導體層所構成，部份的插塞係用以將第一訊號層與第二訊號層電性連接，部份的插塞係用以將第一電壓參考訊號線路與第二電壓參考訊號線路電性連接，而部份的插塞係用以將第二電壓參考訊號線路與第二訊號層電性連接。

本發明具有電壓參考訊號線路佈局之多層基板中，第一訊號層、非訊號層以及第二訊號層各層之間接配置有一介電層，而本發明於第一訊號層外以及第二訊號層外皆配置有一焊罩層。

本發明具有電壓參考訊號線路佈局之多層基板中，在第一訊號層與非訊號層之間可配置一接地-訊號層，而在第二訊號層與非訊號層之間亦可配置一電源-訊號層。

五、發明說明（5）

本發明具有電壓參考訊號線路佈局之多層基板例如係由一訊號層、一非訊號層以及多個插塞所構成。其中，訊號層例如係由一第一電壓參考訊號線路以及多個訊號線路所構成，非訊號層配置於該訊號層下方，非訊號層例如係由一第二電壓參考訊號線路以及一圖案化導體層所構成，而多個插塞配置於訊號層與非訊號層之間，插塞例如係用以將第一電壓參考訊號線路與第二電壓參考訊號線路電性連接。

本發明具有電壓參考訊號線路佈局之多層基板中，訊號層與非訊號層之間配置有一介電層，而訊號層外配置有一焊罩層。

本發明具有電壓參考訊號線路佈局之多層基板中，非訊號層例如係由一接地層以及一電源層。此外，在接地層與電源層之間例如可增加配置至少一層訊號層。

爲讓本發明之上述目的、特徵、和優點能更明顯易懂，下文特舉較佳實施例，並配合所附圖式，作詳細說明如下：

圖式之簡單說明：

第 1 圖繪示爲習知四層板之剖面示意圖；

第 2 圖繪示爲習知訊號層中電壓參考訊號線路佈局的示意圖；

第 3 圖繪示爲習知訊號層中電壓參考訊號線路佈局的示意圖；

第 4 圖繪示爲依照本發明第一實施例四層板之剖面

五、發明說明（6）

示意圖；

第 5 圖繪示爲依照本發明第一實施例訊號層中電壓參考訊號線路佈局的示意圖；

第 6 圖繪示爲依照本發明第一實施例電源層中電壓參考訊號線路佈局的示意圖；

第 7 圖繪示爲依照本發明第一實施例訊號層與電源層重疊之後的電壓參考訊號線路佈局示意圖；

第 8 圖繪示爲依照本發明第二實施例多層板之剖面示意圖；

第 9 圖繪示爲依照本發明第三實施例多層板之剖面示意圖；以及

第 10 圖繪示爲依照本發明第四實施例多層板之剖面示意圖。

圖式之標示說明：

100、200：四層板

102、118、202、218：焊罩層

104、116、204、216：訊號線路層

104a：電壓參考訊號線路

104b、204b：訊號線路

106、110、114、206、210、214：絕緣層

108、208：接地層

112、212：電源層

120、220、222、224：插塞

204a：第一電壓參考訊號線路

五、發明說明（7）

226：第二電壓參考訊號線路

228：圖案化導體層

300：多層板

302、326：焊罩層

304、312、316、324：訊號層

306、310、314、318、322：絕緣層

308：接地層

320：電源層

400：多層板

402、426：焊罩層

404、424：訊號層

406、410、414、418、422：絕緣層

408：接地-訊號層

412：接地層

416：電源層

420：電源-訊號層

500：多層板

502、514：焊罩層

504、512：訊號層

506、510：絕緣層

508：非訊號層

第一實施例

首先請參照第 4 圖，其繪示爲依照本發明第一實施例四層板之剖面示意圖。一般的封裝基板或是印刷電路板

五、發明說明（8）

通常爲一四層板 200。四層板 200 主要是由訊號層 204、接地層 208、電源層 212 以及訊號層 216 所構成。

訊號層 204 與接地層 208 之間配置有絕緣層 206，接地層 208 與電源層 212 之間配置有絕緣層 210，而電源層 212 與訊號層 216 之間配置有絕緣層 214。此外，在訊號層 204 以及訊號層 216 外更配置有焊罩層 202 與焊罩層 218。

訊號層 204 與訊號層 216 中的線路係作爲訊號的輸入/輸出之用，所有的訊號都會由訊號層 204 與訊號層 216 進行輸入/輸出的動作，且訊號層 204 與訊號層 216 之間會藉由插塞（繪示於第 5 圖）而彼此電性連接。

第 5 圖繪示爲依照本發明第一實施例訊號層中電壓參考訊號線路佈局的示意圖。請同時參照第 4 圖以及第 5 圖，訊號層 206、216 中的電壓參考訊號線路佈局主要係由電壓參考訊號線路以及訊號線路所構成。

以位於絕緣層 206 上之訊號層 204 爲例，訊號層 204 中的電壓參考訊號線路佈局例如係由第一電壓參考訊號線路 204a 與多個訊號線路 204b 所構成。其中，第一電壓參考訊號線路 204a 的一端會與一插塞 220 電性連接，而其他的訊號線路 204b 則會分別藉由插塞 224 與下方之訊號層 216 電性連接。

第 6 圖繪示爲依照本發明第一實施例電源層中電壓參考訊號線路佈局的示意圖。請同時參照第 4 圖與第 6 圖，電源層 212 例如係由一第二電壓參考訊號線路 226 以及一

五、發明說明（9）

圖案化導體層 228 所構成。其中，一第二電壓參考訊號線路 226 的兩端例如分別與插塞 220、插塞 222 電性連接，而圖案化導體層 228 例如具有第 6 圖所繪示之圖案化（patterning），圖案化導體層 228 在第二電壓參考訊號線路 226、插塞 220、插塞 222 以及插塞 224 分佈的區域上會呈現簍空的狀態，如此的設計將可以使得圖案化導體層 228 不會與第二電壓參考訊號線路 226、插塞 220、插塞 222、插塞 224 發生短路的現象。

然而，熟習該項技術者應能輕易理解位在訊號層 204 與電源層 212 之間的接地層 208 對應於插塞 220、插塞 222 以及插塞 224 的位置上亦會呈現簍空的狀態，以利插塞 220、插塞 222 以及插塞 224 的配置。

由上述可知，四層板 200 中的插塞 220、插塞 222 以及插塞 224 皆有其作用。其中，插塞 220 例如係將第一電壓參考訊號線路 204a 與第二電壓參考訊號線路 226 電性連接，插塞 220 例如係將第二電壓參考訊號線路 226 與訊號層 216 電性連接，而插塞 224 例如係將訊號層 204 與訊號層 216 電性連接。

第 7 圖繪示爲依照本發明第一實施例訊號層與電源層重疊之後的電壓參考訊號線路佈局示意圖。請同時參照第 4 圖與第 7 圖，將訊號層 204 與電源層 212 重疊之後，可以清楚得知第二電壓參考訊號線路 226 的一端係藉由插塞 220 與第一電壓參考訊號線路 204a 電性連接，而第二電壓參考訊號線路 226 的另一端係藉由插塞 222 與下方的

五、發明說明（\）

訊號層 216 電性連接。

第一電壓參考訊號線路 204a 與第二電壓參考訊號線路 226 係構成一完整的電壓參考訊號線路。由於第二電壓參考訊號線路 226 位於電源層 212 中，而在電源層 212 與訊號層 204 之間的接地層 208 具有電磁遮蔽的效果，這將可大幅的降低電壓參考訊號線路與其他訊號線路之間的耦合雜訊干擾，進一步使得電壓參考訊號線路 204a 中的訊號維持在穩定的電壓準位。

訊號層 204 中的電壓參考訊號線路拉至電源層 212 中進行佈局，進而使得訊號層 204 中的訊號線路 204b 具有較大的佈局空間，而且第二電壓參考訊號線路 226 本身也會具有相當大的佈局彈性。此外，第二電壓參考訊號線路 226 可採用寬導線的設計以改善其寄生電阻的問題。

然而，熟習該項技術者應能輕易的瞭解，將訊號層 204 中的電壓參考訊號線路拉至接地層 208 中進行佈局亦爲一可行的方式。這樣的佈局同樣能夠增加訊號線路 204b 的佈局空間以及電壓參考訊號線路本身的佈局彈性。

第二實施例

請參照第 8 圖，其繪示爲依照本發明第二實施例多層板之剖面示意圖。本發明電壓參考訊號線路的佈局觀念並非只能應用於四層板中，其亦可應用於多層板中。本實施例中，多層板 300 主要是由訊號層 304、接地層 308、訊號層 312、訊號層 316、電源層 320 以及訊號層 324 所構成。訊號層 304 與接地層 308 之間配置有絕緣層 306，

五、發明說明（12）

接地層 308 與訊號層 312 之間配置有絕緣層 310，訊號層 312 與訊號層 316 之間配置有絕緣層 314，訊號層 316 與電源層 320 之間配置有絕緣層 318，而電源層 320 與訊號層 324 之間配置有絕緣層 322。此外，在訊號層 304 以及訊號層 324 外更配置有焊罩層 302 與焊罩層 326。

本實施例中，可將訊號層 304 中的電壓參考訊號線路拉至接地層 308 或電源層 320 中進行佈局，如此同樣能夠達到避免耦合雜訊干擾、增進佈局彈性的目的。

第三實施例

請參照第 9 圖，其繪示爲依照本發明第三實施例多層板之剖面示意圖。本實施例中，多層板 400 主要是由訊號層 404、接地-訊號層 408、接地層 412、電源層 416、電源-訊號層 420 以及訊號層 424 所構成。訊號層 404 與接地-訊號層 408 之間配置有絕緣層 406，接地-訊號層 408 與接地層 412 之間配置有絕緣層 410，接地層 412 與電源層 416 之間配置有絕緣層 414，電源層 416 與電源-訊號層 420 之間配置有絕緣層 418，而電源-訊號層 420 與訊號層 424 之間配置有絕緣層 422。此外，在訊號層 404 以及訊號層 424 外更配置有焊罩層 402 與焊罩層 426。

本實施例中，可將訊號層 404 中的電壓參考訊號線路拉至接地-訊號層 408、接地層 412、電源層 416 或是電源-訊號層 420 中進行佈局，以期能夠達到避免耦合雜訊干擾、增進佈局彈性的目的。

第四實施例

五、發明說明（17）

請參照第 10 圖，其繪示爲依照本發明第四實施例多層板之剖面示意圖。本實施例中，多層板 500 主要是由訊號層 504、非訊號層 508 以及訊號層 512 所構成。訊號層 504 與非訊號層 508 之間配置有絕緣層 506，而非訊號層 508 與訊號層 512 之間配置有絕緣層 510。此外，在訊號層 504 以及訊號層 512 外更配置有焊罩層 502 與焊罩層 514。

本實施例中，可將訊號層 504 中的電壓參考訊號線路拉至非訊號層 508 中進行佈局，以期能夠達到避免耦合雜訊干擾、增進佈局彈性的目的。

綜上所述，本發明具有電壓參考訊號線路佈局之多層基板至少具有下列優點：

1.本發明具有電壓參考訊號線路佈局之多層基板中，電壓參考訊號線路可藉由接地層的電磁遮蔽效果，進而大幅的降低電壓參考訊號線路與其他訊號線路之間的耦合雜訊干擾。

2.本發明具有電壓參考訊號線路佈局之多層基板中，電壓參考訊號線路配置於信號層以外之導線層中，使得電壓參考訊號線路本身的佈局彈性大增。

3.本發明具有電壓參考訊號線路佈局之多層基板中，電壓參考訊號線路配置於信號層以外之導線層中，使得其他訊號線路在訊號層中有較大的佈局空間。

4.本發明具有電壓參考訊號線路佈局之多層基板中，電壓參考訊號線路配置於信號層以外之導線層中，可將電壓參考訊號線路設計爲較寬的導線，以有效的降低導線上

五、發明說明（14）

的寄生電阻。

雖然本發明已以較佳實施例揭露如上，然其並非用以限定本發明，任何熟習此技藝者，在不脫離本發明之精神和範圍內，當可作各種之更動與潤飾，因此本發明之保護範圍當視後附之申請專利範圍所界定者爲準。

六、申請專利範圍

1.一種具有電壓參考訊號線路佈局之多層基板，包括：

一第一訊號層，該第一訊號層包括一第一電壓參考訊號線路以及複數個訊號線路；

一第二訊號層，配置於第一訊號層下方；

複數個第一插塞，配置於該第一訊號層與該第二訊號層之間，並將該些訊號線路與該第二訊號層電性連接；

一接地層，配置於該第一訊號層與該第二訊號層之間；

一電源層，配置於該第一訊號層與該第二訊號層之間，該電源層包括一第二電壓參考訊號線路以及一圖案化導體層；

一第二插塞，配置於該電源層與該第一訊號層之間，並將該第一電壓參考訊號線路與該第二電壓參考訊號線路電性連接；以及

一第三插塞，配置於該電源層與該第二訊號層之間，並該第二電壓參考訊號線路與該第二訊號層電性連接。

2.如申請專利範圍第 1 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第一訊號層、該接地層、該電源層以及該第二訊號層各層之間配置有一介電層。

3.如申請專利範圍第 1 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第一訊號層外配置有一第一焊罩層。

4.如申請專利範圍第 1 項所述之具有電壓參考訊號線

六、申請專利範圍

路佈局之多層基板，其中該第二訊號層外配置有一第二焊罩層。

5.如申請專利範圍第 1 項所述之具有電壓參考訊號線路佈局之多層基板，其中該接地層與該電源層之間更配置有一第三訊號層。

6.如申請專利範圍第 5 項所述之具有電壓參考訊號線路佈局之多層基板，其中該接地層與該電源層之間更配置有一第四訊號層。

7.如申請專利範圍第 1 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第一訊號層與該接地層之間更配置有一接地-訊號層。

8.如申請專利範圍第 1 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第二訊號層與該電源層之間更配置有一電源-訊號層。

9.如申請專利範圍第 1 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第一訊號層與該接地層之間更配置有一接地-訊號層，且該第二訊號層與該電源層之間更配置有一電源-訊號層。

10.一種具有電壓參考訊號線路佈局之多層基板，包括：

一第一訊號層，該第一訊號層包括一第一電壓參考訊號線路以及複數個訊號線路；

一第二訊號層，配置於該第一訊號層下方；

複數個第一插塞，配置於該第一訊號層與該第二訊

六、申請專利範圍

號層之間，並將該些訊號線路與該第二訊號層電性連接；

至少一非訊號層，配置於該第一訊號層與該第二訊號層之間，該非訊號層包括一第二電壓參考訊號線路以及一圖案化導體層；

一第二插塞，配置於該非訊號層與該第一訊號層之間，並將該第一電壓參考訊號線路與該第二電壓參考訊號線路電性連接；以及

一第三插塞，配置於該非訊號層與該第二訊號層之間，並該第二電壓參考訊號線路與該第二訊號層電性連接。

11.如申請專利範圍第 10 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第一訊號層、該非訊號層以及該第二訊號層各層之間配置有一介電層。

12.如申請專利範圍第 10 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第一訊號層外配置有一第一焊罩層。

13.如申請專利範圍第 10 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第二訊號層外配置有一第二焊罩層。

14.如申請專利範圍第 10 項所述之具有電壓參考訊號線路佈局之多層基板，其中該非訊號層包括一電源層。

15.如申請專利範圍第 14 項所述之具有電壓參考訊號線路佈局之多層基板，其中該非訊號層包括一接地層。

16.如申請專利範圍第 15 項所述之具有電壓參考訊號

六、申請專利範圍

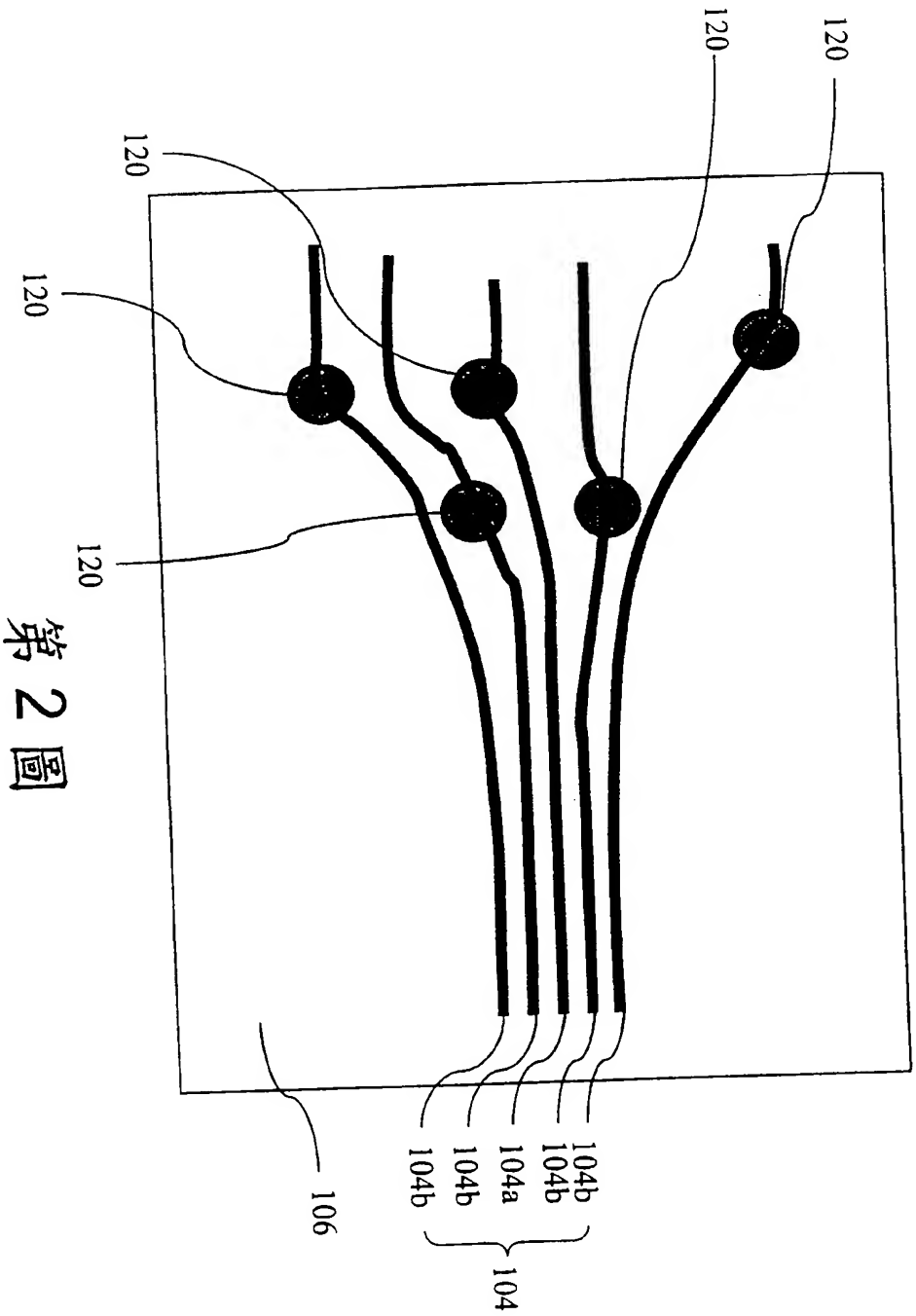
線路佈局之多層基板，其中該接地層與該電源層之間更配置有一第三訊號層。

17.如申請專利範圍第 15 項所述之具有電壓參考訊號線路佈局之多層基板，其中該接地層與該電源層之間更配置有一第四訊號層。

18.如申請專利範圍第 10 項所述之具有電壓參考訊號線路佈局之多層基板，其中第一訊號層與該非訊號層之間更配置有一接地-訊號層。

19.如申請專利範圍第 10 項所述之具有電壓參考訊號線路佈局之多層基板，其中該第二訊號層與該非訊號層之間更配置有一電源-訊號層。

第 1 圖



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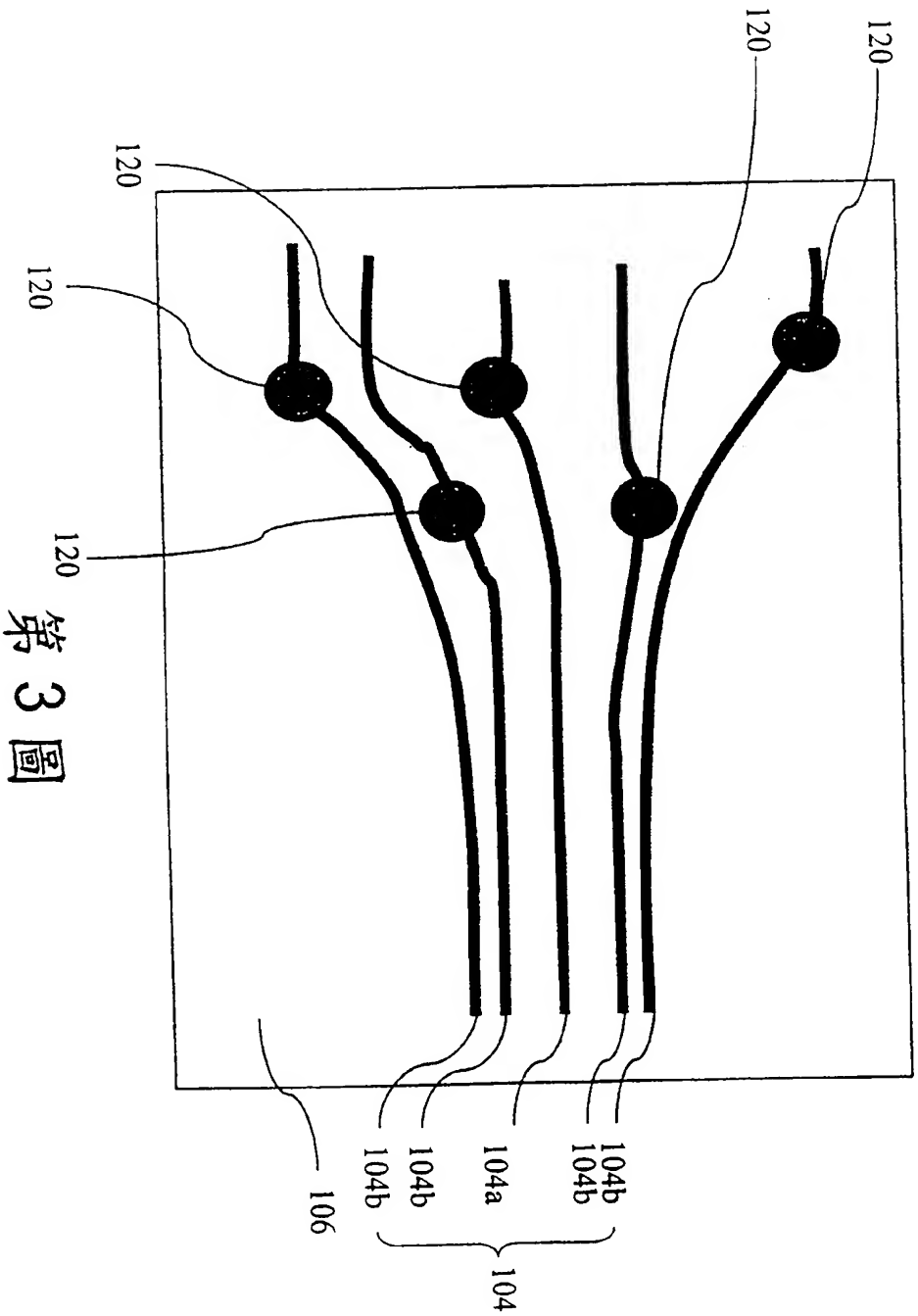

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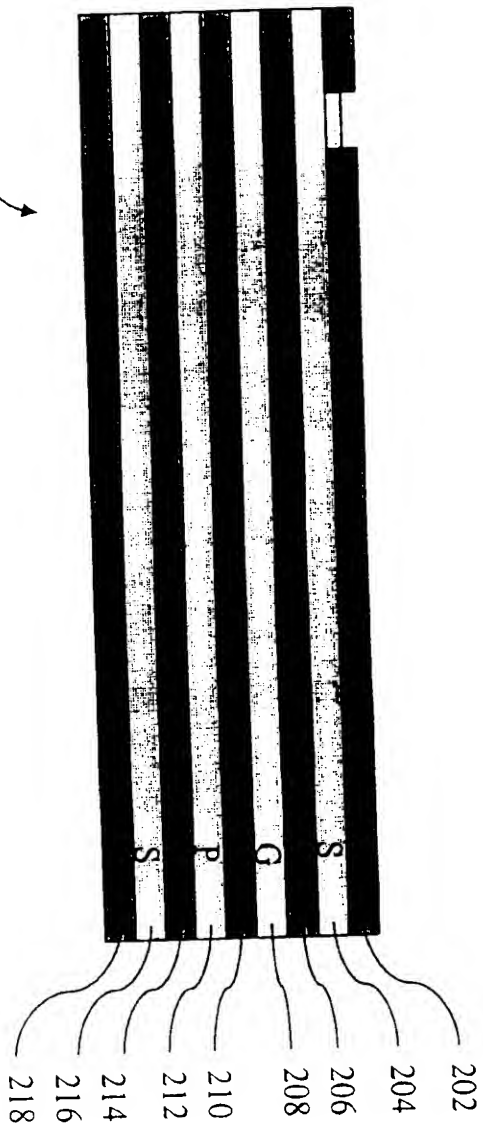

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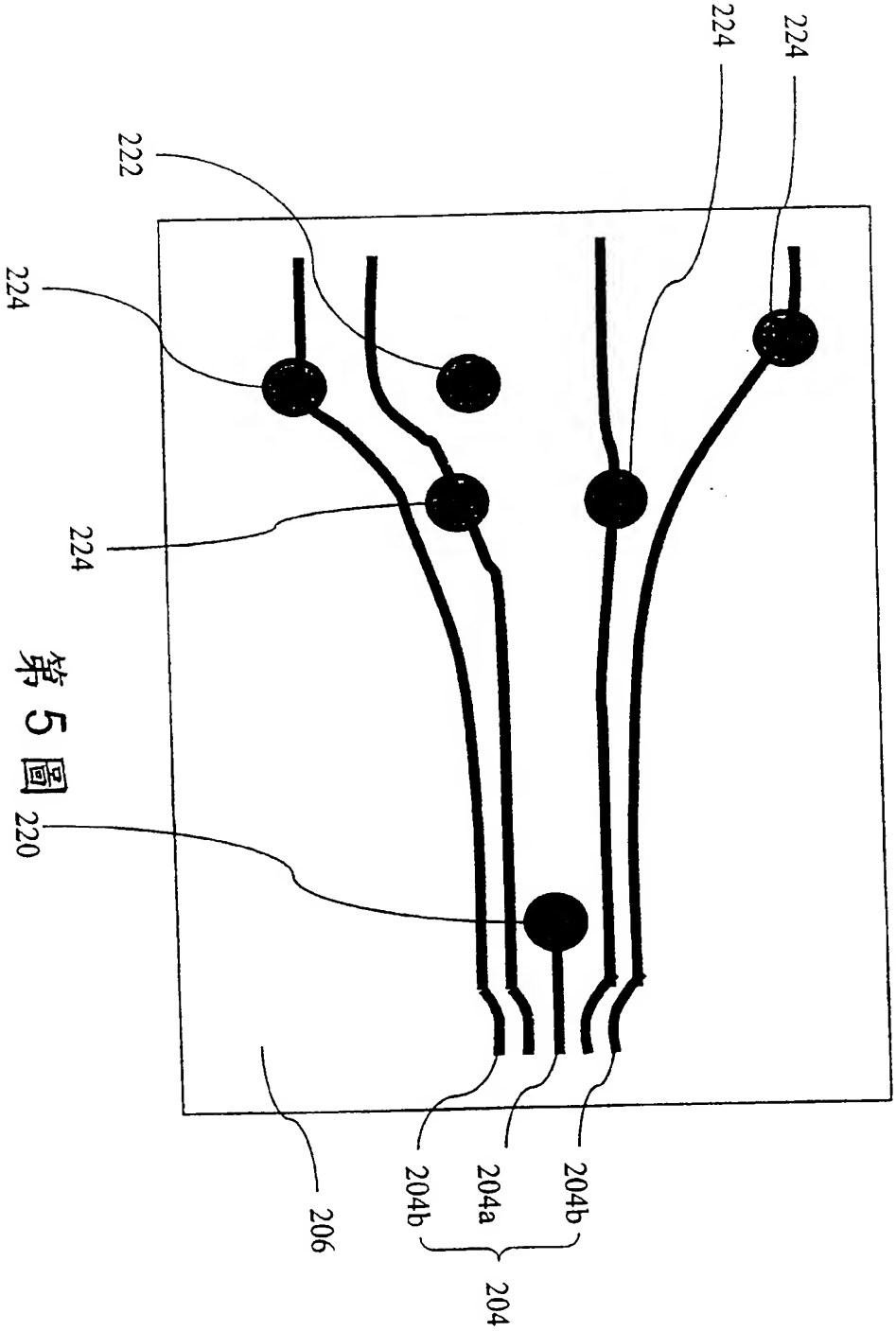

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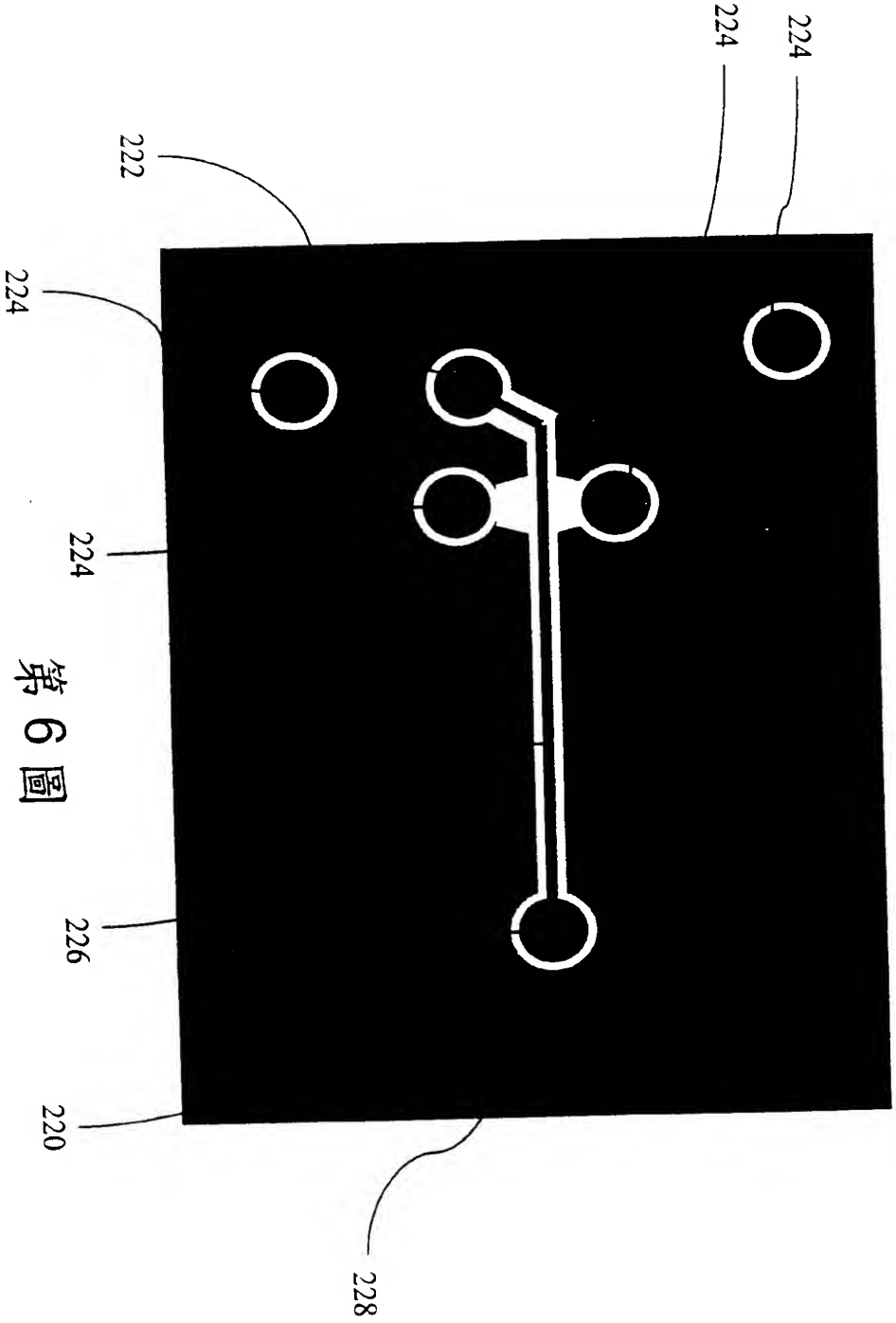

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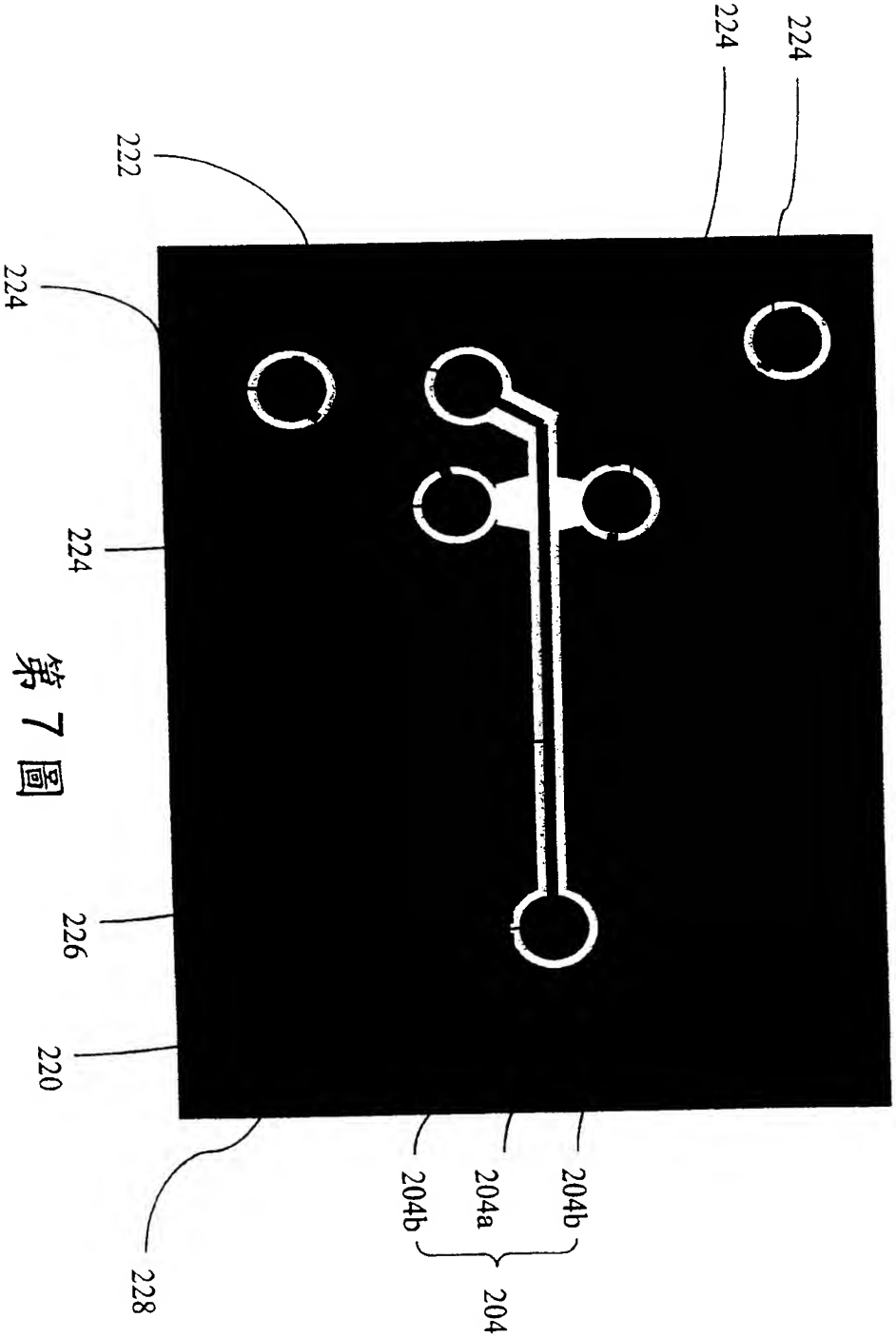

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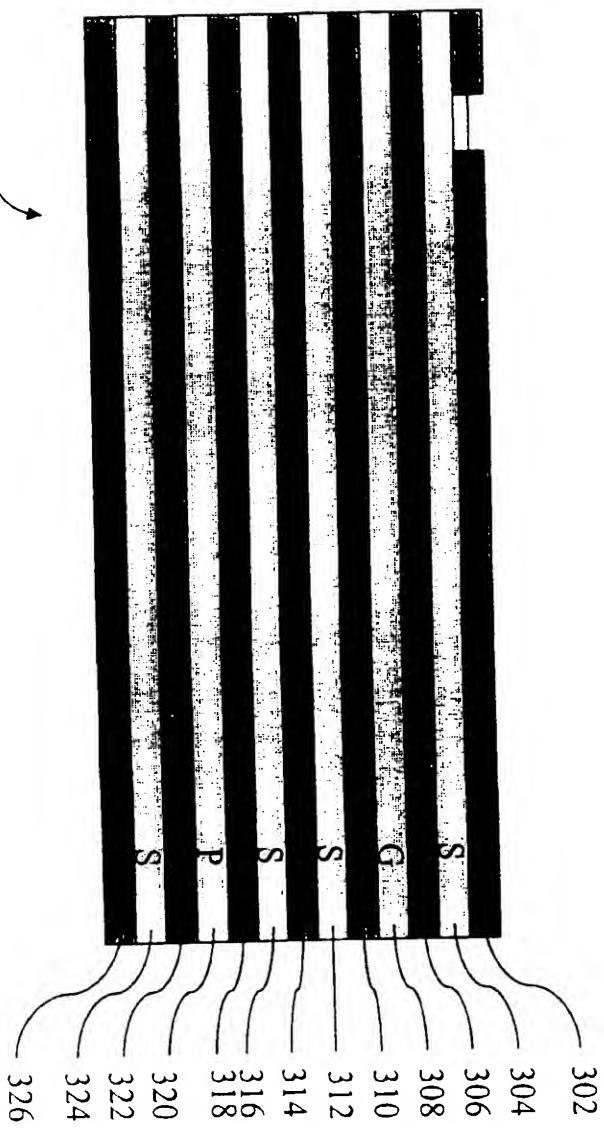

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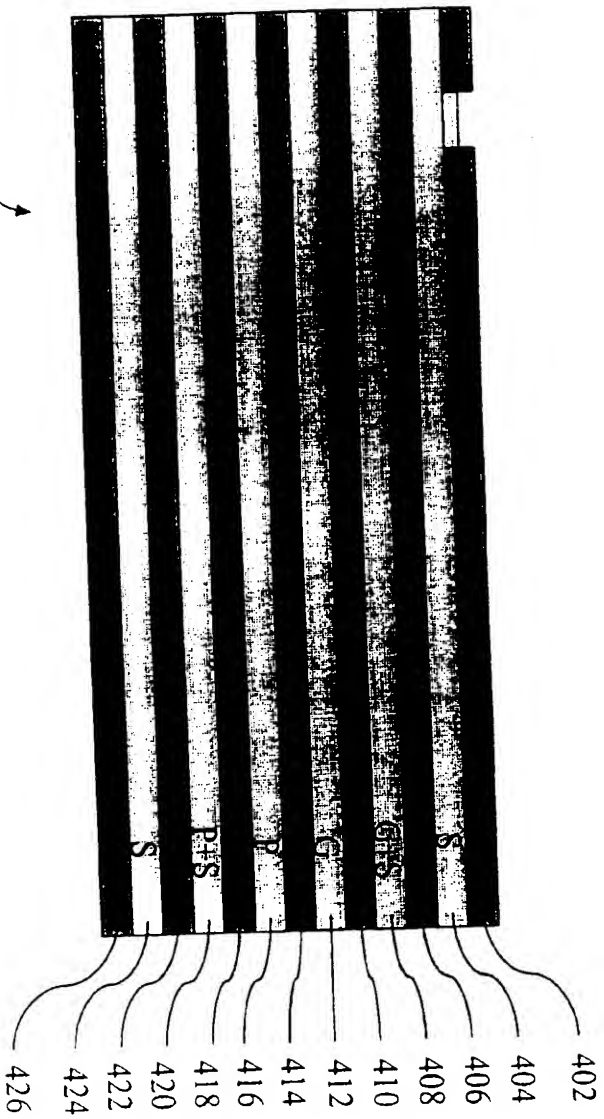
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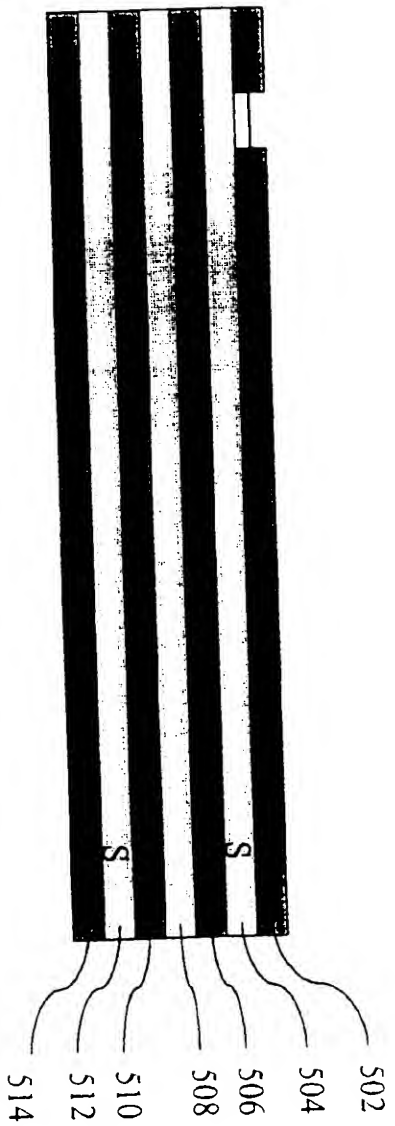
第 9 圖



第 10 圖